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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/529,163	12/30/2003	Arkady Molev-Shteiman	968/32	1595

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EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/529,163	MOLEV-SHTEIMAN, ARKADY	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 have been presented for examination.

PRIORITY

2. Acknowledgment is made of applicant's claim for priority to PCT/US98/19708 filed on 09/18/1998 which is a continuation of 08/947,467 filed on 10/09/1997.

Examiner's Interpretation

3. Examiner interprets claims 1-6 in light of the specification of the limitation "As each new input bit arrives, the contents of the shift register are shifted over one bit to accommodate the new input bit. Note that this automatically discards the old input bit that preceded the new input bit by K bits." **(page 1, lines 19-21)**. If the claims are not interpreted in this light, then the claims will be rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims will not contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Without interpretation in light of the specification, the method will attempt to fit an updated word which will be j bits plus the length of the original word into the shift and RAM registers where the shift and RAM registers only have the ability to hold the original word. Claims 3-4 will have similar 112, 1st issues if not interpreted in light of the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at

the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Jan et al. (U.S. Patent No. 5,479,128) in view of Dixon et al. (U.S. Patent No. 5,568,443).**

As per claim 1, Jan is directed to a method of processing successive input bits providing a RAM array which replaces the series of individual registers **(column 1, lines 40-43)** and emulates the registers, each of the registers storing a word **(column 1, lines 40-43)**, all of said words being of equal length (ii) a shift register at least as long as any of said words **(column 4, lines 32-35)** and (c) for each group of j input bits shorter than said words: (i) writing said word, stored in said register, to said shift register **(column 3, lines 57-62)**, (ii) shifting said word in said shift register by j bits **(column 3, lines 45-55)**, (iii) writing said group of j input bits to said shift register, thereby producing an updated word in said shift register **(column 3, lines 45-55)**, (iv) storing said updated word in said register **(column 3, lines 57-62)** but does not explicitly disclose a pointer to point to the RAM registers.

Dixon teaches (a) providing a pointer **(column 6, lines 1-3)**, (b) initializing said pointer to point to one of said registers of said RAM **(column 6, lines 1-3)**; and (v) incrementing said pointer **(column 5, lines 34-39)**.

Jan and Dixon are analogous art because they are both from the same field of endeavor, processing successive input bits. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the shift register emulation method of Jan with the input memory method of Dixon in order to reduce cost, power consumption, and board space **(Dixon, column 1, lines 22-28)**.

As per claim 2, the combination of Jan and Dixon already discloses the method of claim 1, wherein j equals 1. Although the combination of Jan Dixon do not explicitly disclose the method of claim 1 wherein j equals 1, it would be obvious to one of ordinary skill in the art at the time of the invention to have a single bit delay in order to generate lower range value delays.

As per claim 3, the combination of Jan and Dixon already discloses the method of claim 1, wherein all of said registers of said RAM are as long as each of said words **(Jan, column 3, lines 16-20)**.

As per claim 4, the combination of Jan and Dixon already discloses the method of claim 1, wherein said shift register is as long as each of said words **(Jan, column 3, lines 32-35)**.

As per claim 5, the combination of Jan and Dixon already discloses the method of claim 1, further comprising the step of:

(d) successively reading and processing at least some of said words stored in said registers of said RAM **(Jan, column 4, lines 13-15)**.

As per claim 6, the combination of Jan and Dixon already discloses the method of claim 5, wherein all of said words stored in said registers of said RAM are read successively and processed **(Jan, column 4, lines 13-15)**.

Conclusion

5. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 5,406,518 issued to Sun et al. on 04/11/95.

2. U.S. Patent No. 4,548,134 issued to Wadley et al. on 10/22/85.

3. "The automated generation of cross-system software for supporting micro/mini computer systems" published by Johnson et al. in 1976.

4. "A FPGA ASIC communication channel systems emulator" published by Page et al. in 1993.

7. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
05/19/06

KAMINI SHAH
SUPERVISORY PATENT EXAMINER